DATA SHEET

TDA8380A
Control circuit for switched mode power supplies

Product specification
Supersedes data of October 1993
File under Integrated Circuits, IC02

November 1993

Philips Semiconductors





Control circuit for switched mode power supplies TDA8380A

GENERAL DESCRIPTION

The TDA8380A is an integrated circuit intended for use as a control circuit in low-cost switched mode power supplies for television, monitors and small industrial equipment. The TDA8380A operates using duty factor regulation in the fixed frequency mode.

Features

- A low-current initialization circuit (maximum 150 μA) which can be switched off
- A bandgap reference generator
- Circuitry for slow-start combined with an accurate setting of the maximum duty factor (D_{max})
- Programmable low supply voltage protection with one default value
- High supply protection circuitry
- Error amplifier with a transfer characteristic generator (TCG)
- Protection against open- and short-circuited feedback loop
- An overload voltage foldback
- Primary current protection circuitry for both cycle-by-cycle and trip mode
- Protection against transformer saturation
- A direct drive output stage (sink current 2.5 A, source current 0.75 A)
- Anti-double pulse logic
- Protected against damage as a result of a short-circuited high-voltage transistor
- RC oscillator with synchronization input

QUICK REFERENCE DATA

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	–	14	–	V
Supply current	I_{CC}	–	–	15	mA
Output pulse repetition frequency range	f_o	10	–	100	kHz
Operating ambient temperature range	T_{amb}	–25	–	+ 70	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38); SOT38-1 ; 1996 November 18.

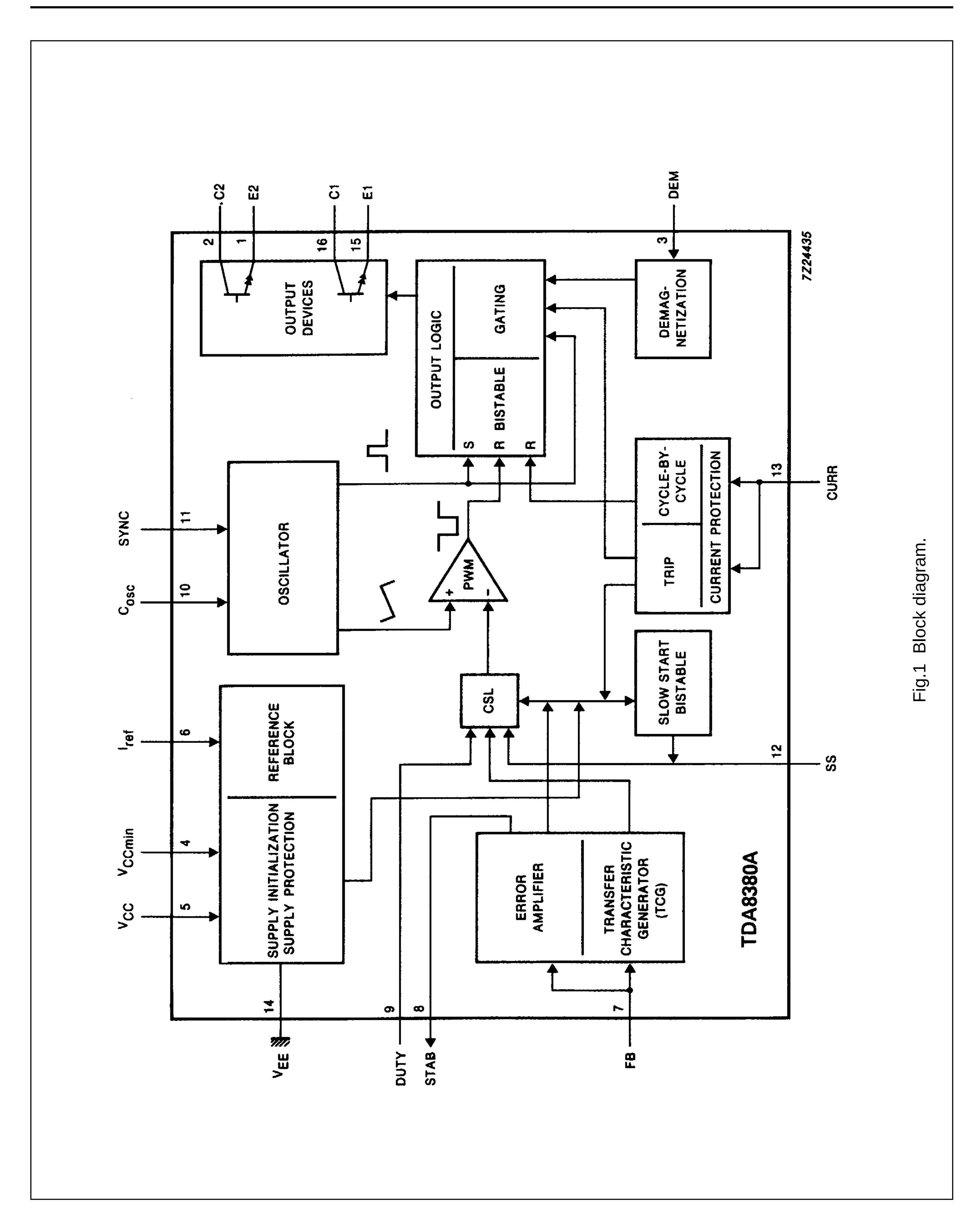


Fig.1 Block diagram.

PINNING

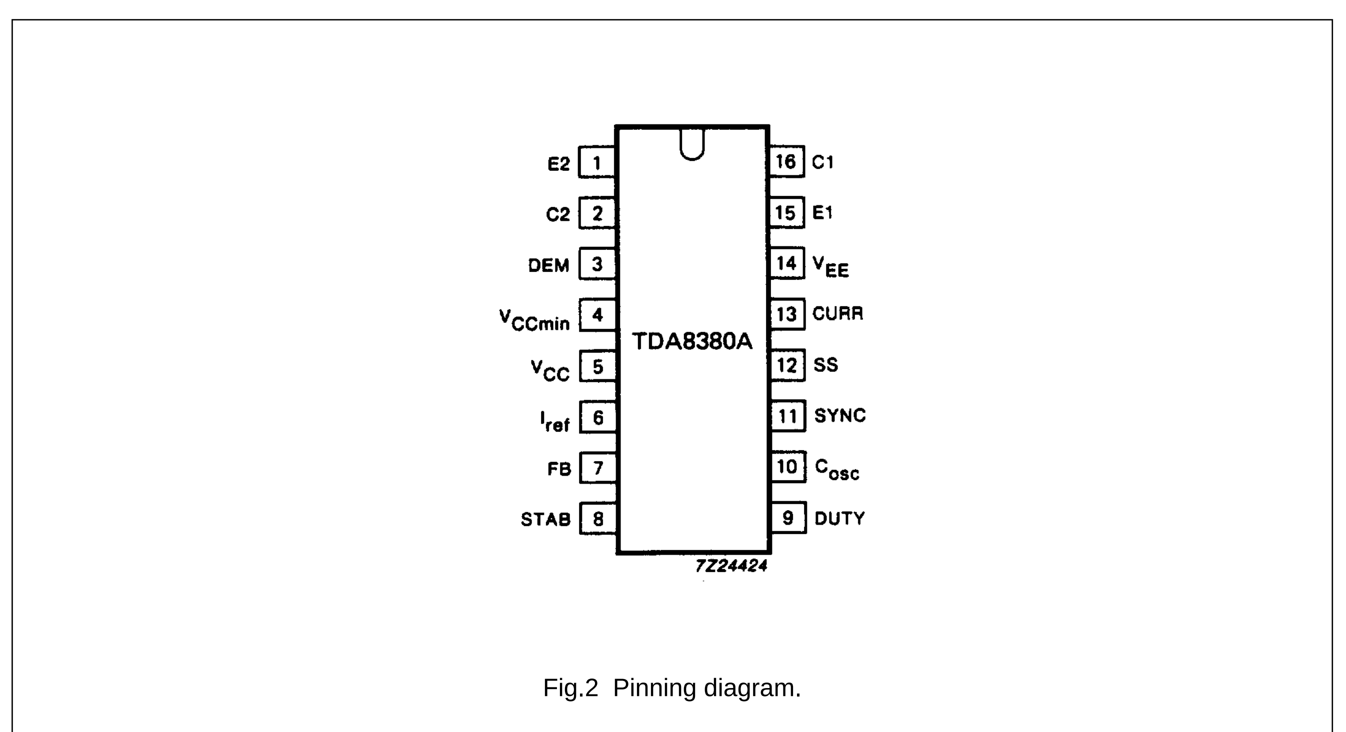


Fig.2 Pinning diagram.

1	E2	Emitter of output source transistor
2	C2	Collector of output source transistor
3	DEM	Demagnetization sense input
4	V_{CCmin}	Minimum V_{CC} threshold setting
5	V_{CC}	Supply voltage
6	I_{ref}	Reference current setting
7	FB	Feedback input
8	STAB	Output error amplifier
9	DUTY	Pulse width modulator input
10	C_{OSC}	Oscillator capacitor
11	SYNC	Synchronization input
12	SS	Maximum duty factor (D_{max}) setting plus slow-start
13	CURR	Input current protection
14	V_{EE}	Ground
15	E1	Emitter of output sink transistor
16	C1	Collector of output sink transistor

FUNCTIONAL DESCRIPTION

The TDA8380A is a control circuit which generates the pulses required to drive the switching transistor in a switched mode power supply (SMPS).

Supply

This device is intended to be used on the primary side of the power supply and can be supplied via a take-over (auxiliary) winding on the transformer.

The device is initialized via a high value resistor connected between the rectified mains voltage and the device's supply pin (pin 5), which causes the capacitor connected to this pin to charge slowly. When the voltage exceeds the initialization level (typically 17 V) the device will start up and the duty cycle will be slowly increased by the slow-start circuit. After a short period the take-over winding will supply the device. The value of the resistor is normally defined by the time taken to charge the capacitor.
A one second delay between switching on and operation of the power supply is acceptable in most cases.

The operating voltage range is from 9 to 20 V. The supply pin is protected by a 23 V Zener diode. The supply protection circuit is activated once the Zener diode is conducting. The slow-start procedure begins after initialization, until then the output is off. The current drawn by the device during the initialization period is less than 150 µA.

When the supply voltage falls below the minimum trip level, the device switches off and the start-up procedure is repeated. The minimum voltage supply threshold setting (V_{CCmin}) can be set externally with a resistor connected between the V_{CCmin} pin (pin 4) and ground (pin 14) (see Fig.3).

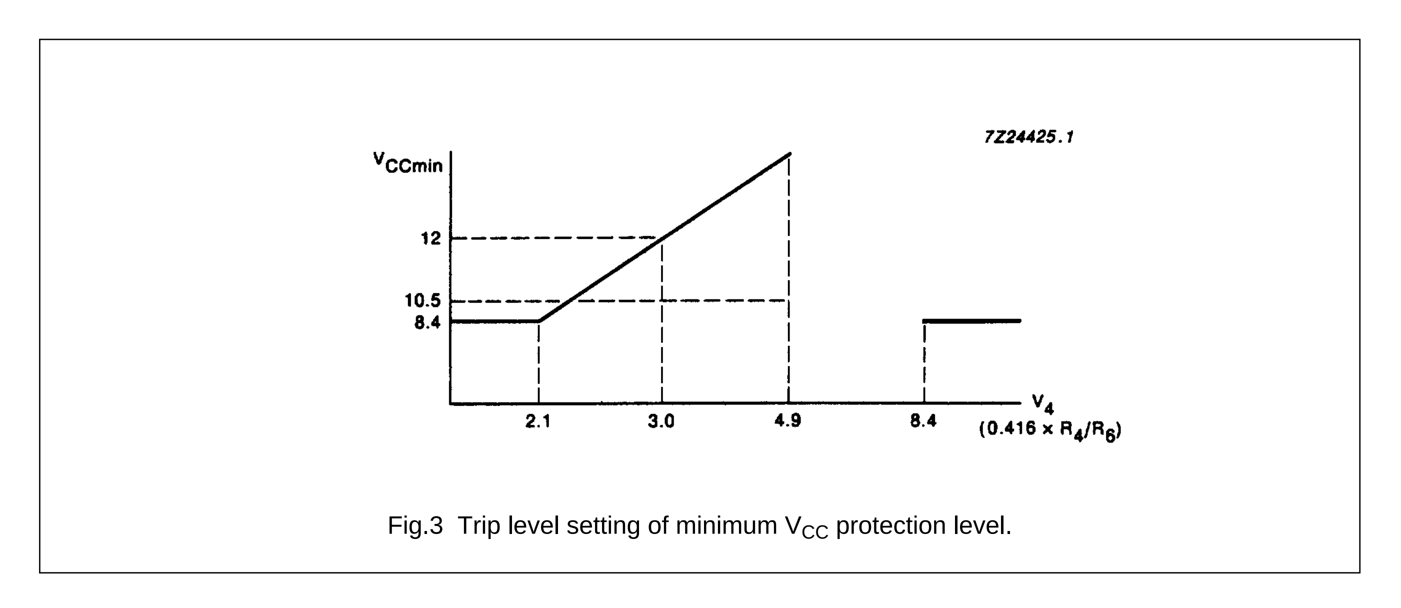


Fig.3 Trip level setting of minimum V_{CC} protection level.

V_{CCmin} can be set between 8.4 V (an internally fixed overriding protection level) and 17 V by means of an external resistor connected to pin 4.

When choosing the initialization and minimum supply voltages the following should be taken into account:

- The difference between the two voltages should be large enough to enable a supply voltage dip during start-up.
- The value of the minimum supply voltage should be high enough to ensure that the high-voltage transistor is correctly driven. A high protection level makes it possible to have a large resistor value in series with the base drive.

For battery line input operation, the V_{CCmin} pin is connected to V_{CC}, the start-up circuit is then inhibited and the device starts operating when V_{CC} exceeds the 8.4 V protection level (this level has a hysteresis of approximately 50 mV). The device draws current continuously under these conditions.

Reference block

A bandgap based reference generates a stabilized voltage of 7 V to supply most of the device's internal circuits, this decreases chip size and increases reliability. The only circuits connected to V_{CC} are:

- The initialization circuit
- The output circuitry
- The series transistor of the stabilized voltage

By means of a resistor (R_6) connected to the I_{ref} input a reference current is defined which determines six other device settings.

Part of the reference current is used to charge the oscillator capacitor (C_{10}), therefore, the charging time is proportional to $R_6 \times C_{10}$. The maximum duty factor (D_{max}) is set by the resistor connected to pin 12 (R_{12}) and is defined by the ratio R_6/R_{12}. The minimum supply voltage (pin 5) set by the resistor (R_4) at input V_{CCmin} is defined by: $4/6 \times V_6 \times R_4/R_6$.

Oscillator

The oscillator capacitor is charged and discharged between the high and low voltage levels as defined by the bandgap reference (high voltage typically 5 V and low voltage typically 1.4 V). The charge current is 1/6 of the reference current, the discharge current having the same value as the reference current. The period is therefore defined by $10 \times R_6 \times C_{10}$.

The oscillator flyback pulse is used to set the bistable in the output logic, however the output remains low until the positive ramp starts (see Fig.4). The oscillator can be synchronized by means of the SYNC pin. When this pin is connected to V_{CC}, the oscillator is free running. When it is between 0.85 and 5.6 V, the oscillator stops at the low voltage level prior to the next positive ramp.

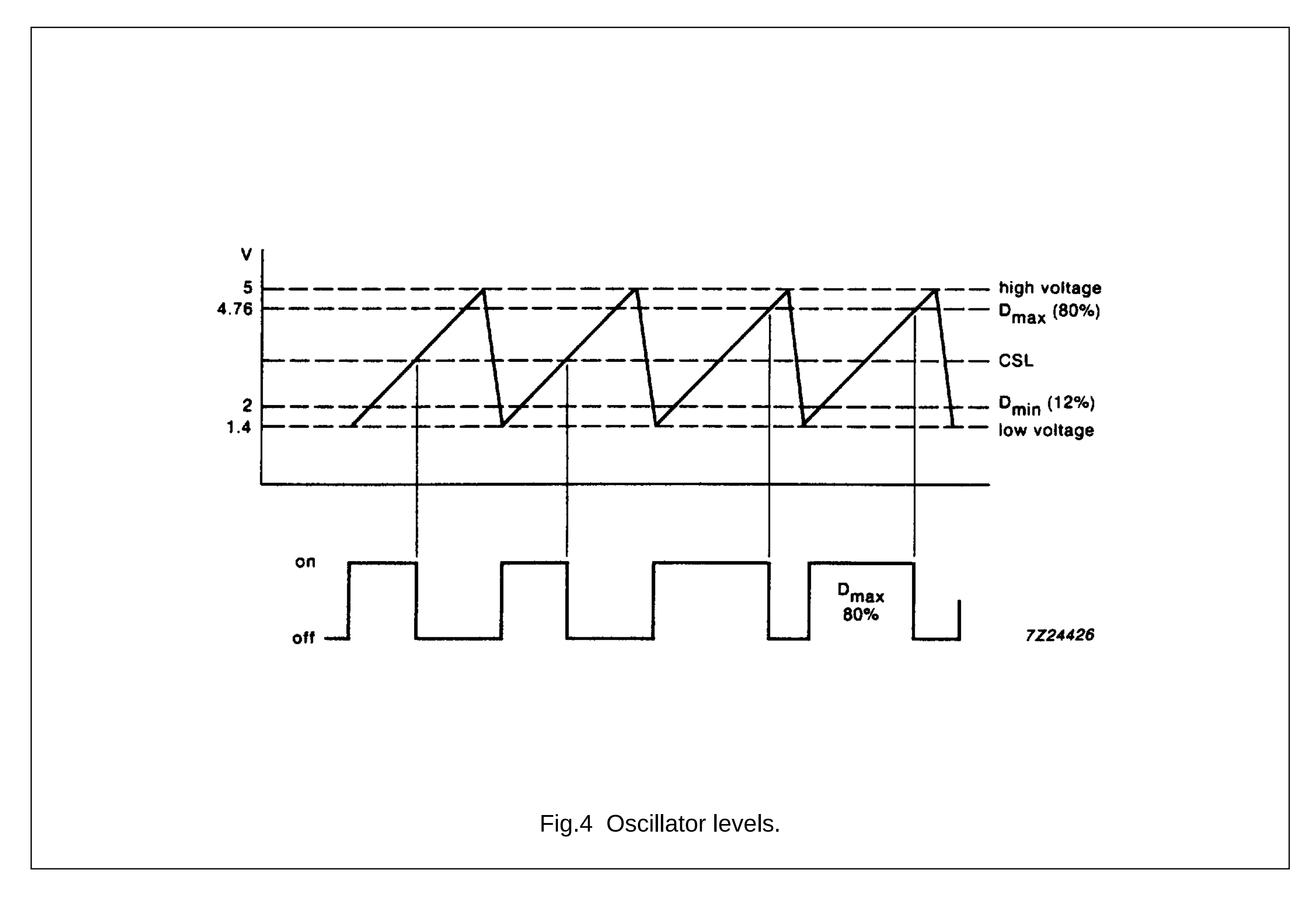


Fig.4 Oscillator levels.

Synchronization

The synchronisation input (pin 11) can be driven by either an optocoupler or a loosely coupled pulse transformer.

Figure 5 illustrates synchronization using the 0.85 V threshold and a digital signal connected to the SYNC input (for example, an optocoupler between pin 11 and V_{CC}); the duty factor of the pulse is not very important. The oscillator starts at the first negative going edge of the sync. signal after the low voltage level has been reached. The synchronization frequency must be lower than the free running frequency. Synchronization must never affect the period time as this will corrupt the setting of the maximum duty factor.

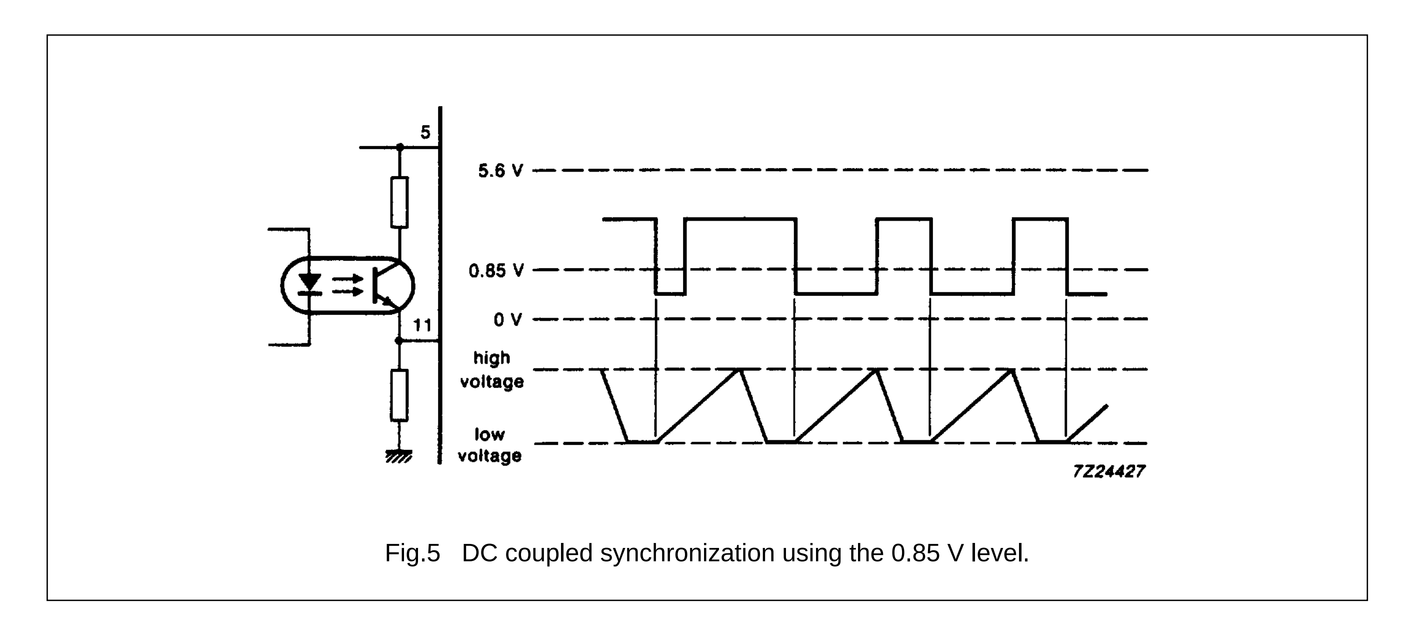


Fig.5 DC coupled synchronization using the 0.85 V level.

In Fig.6 the disabling threshold (5.6 V) is used for synchronization. In this case the oscillator starts at the positive going edge of the sync. signal.

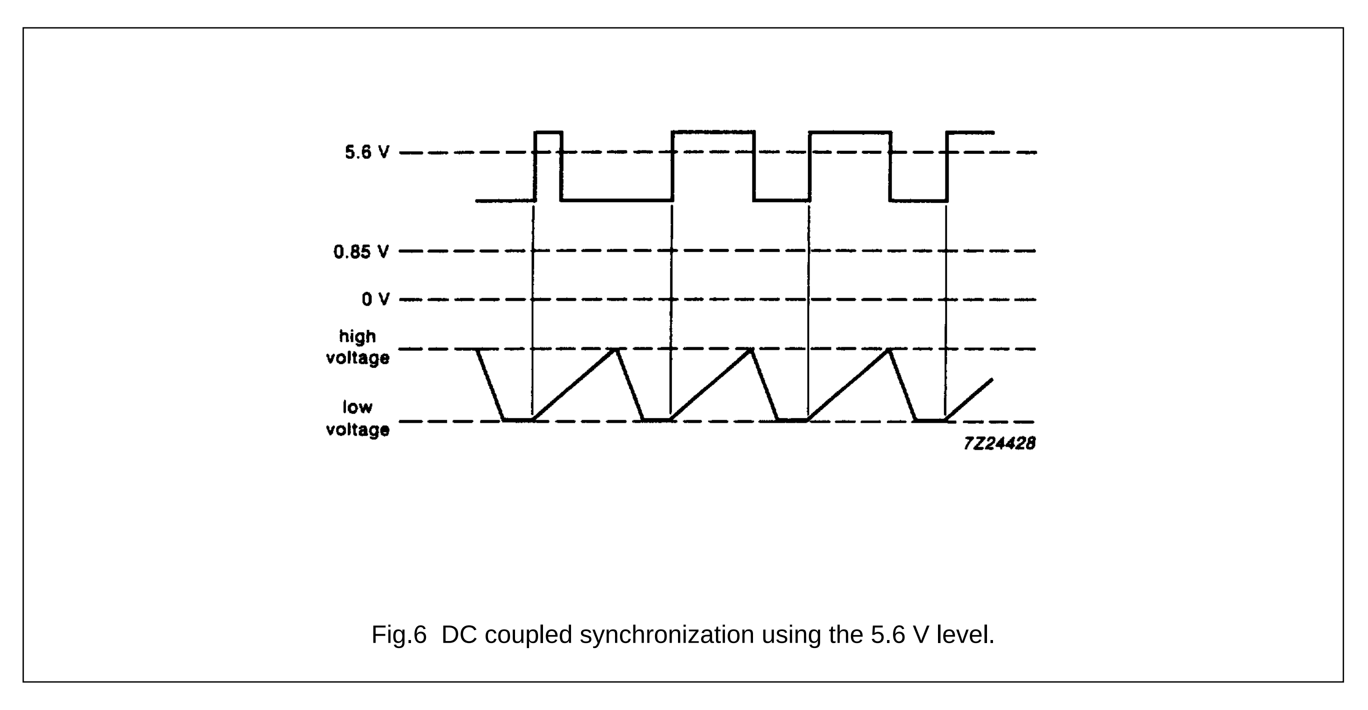


Fig.6 DC coupled synchronization using the 5.6 V level.

Figure 7 illustrates synchronization using a pulse transformer. Internal circuitry causes a DC shift which informs the device that synchronization pulses are present (spikes around 0 V at the output of the pulse transformer) or not present (DC 0 V at the output of the pulse transformer). When synchronization is not used the SYNC pin must be connected to V_{CC}, it must not be connected directly to ground or left open.

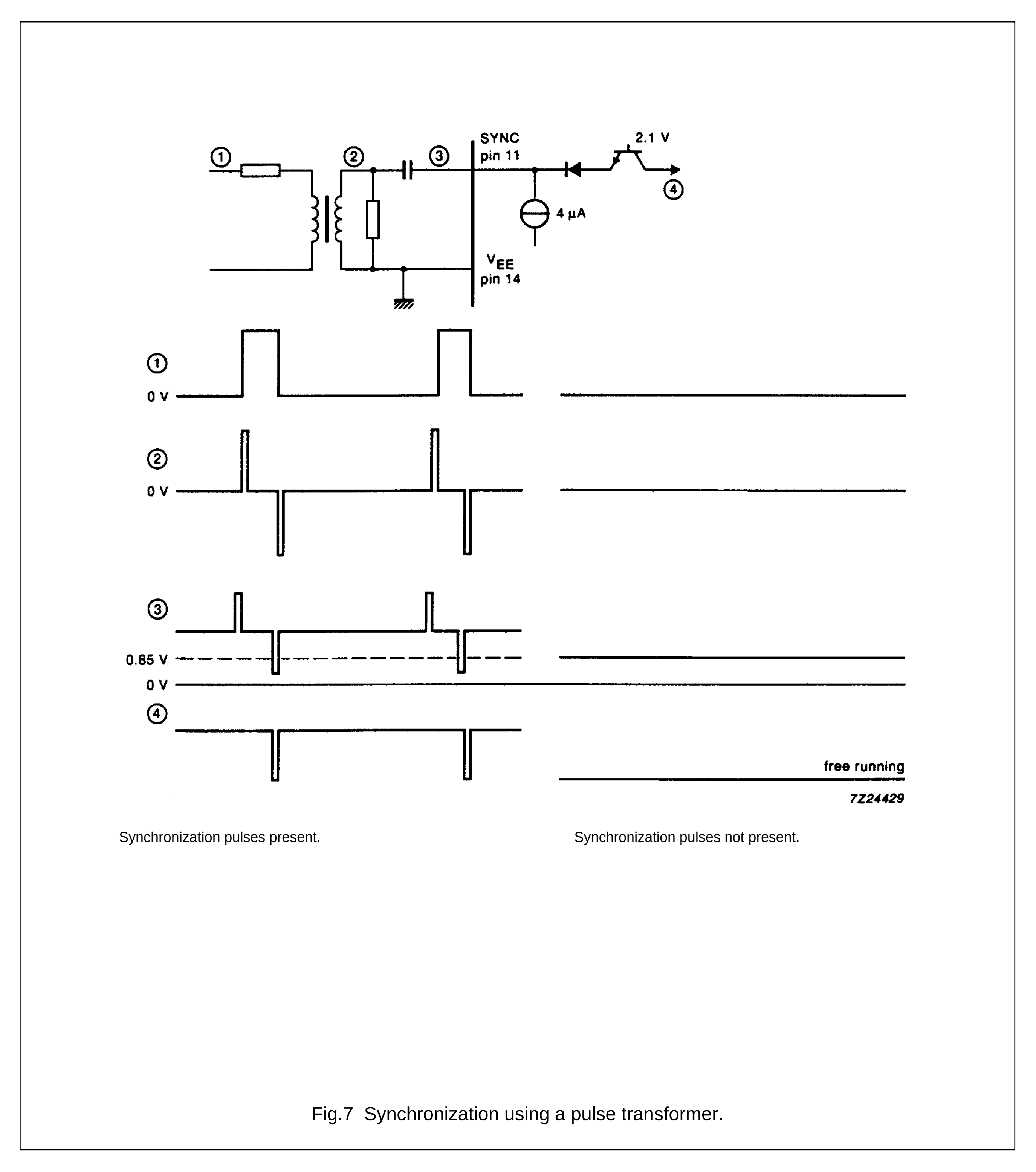


Fig.7 Synchronization using a pulse transformer.

Error amplifier

The error amplifier compares the feedback voltage of the SMPS with a reference voltage (nominally 2.5 V). The amplifier output at pin 8 enables gain setting. The amplifier is stable for a gain greater than 20 dB.

The output of the error amplifier is not internally connected to the Pulse Width Modulator (PWM). One input to the PWM is available at the DUTY input (pin 9) via the Control Slicing Level (CSL) circuit. Normally the STAB and DUTY pins are connected together, but direct driving of pin 9 via an optocoupler from the secondary side is also possible. A type of current mode control can be achieved by mixing the STAB signal with the primary current signal before applying it to the DUTY input.

The feedback (FB) input (pin 7) is used as the input to the Transfer Characteristic Generator (TCG) circuit which ensures well defined duty factors at low FB voltages; a voltage foldback is an inherent characteristic. In Fig.8, the duty factor is shown as a function of the voltages at the FB, DUTY and SS inputs. The input which gives the lowest duty factor overrides the others.

The left hand curve is passed through during a slow-start (via the slow-start input pin 12) when the duty cycle slowly increases linearly with respect to V_{12}. The right-hand curve is passed through at start-up. The FB voltage slowly increases from zero and the duty factor, starting at 12%, increases until the maximum duty factor (D_{max}) is reached. A few hundred millivolts later, the FB voltage reaches the start of the regulation curve which is at approximately 2.5 V. The plateau area between reaching D_{max} and starting the regulation curve is kept as small as possible (typically 200 mV).

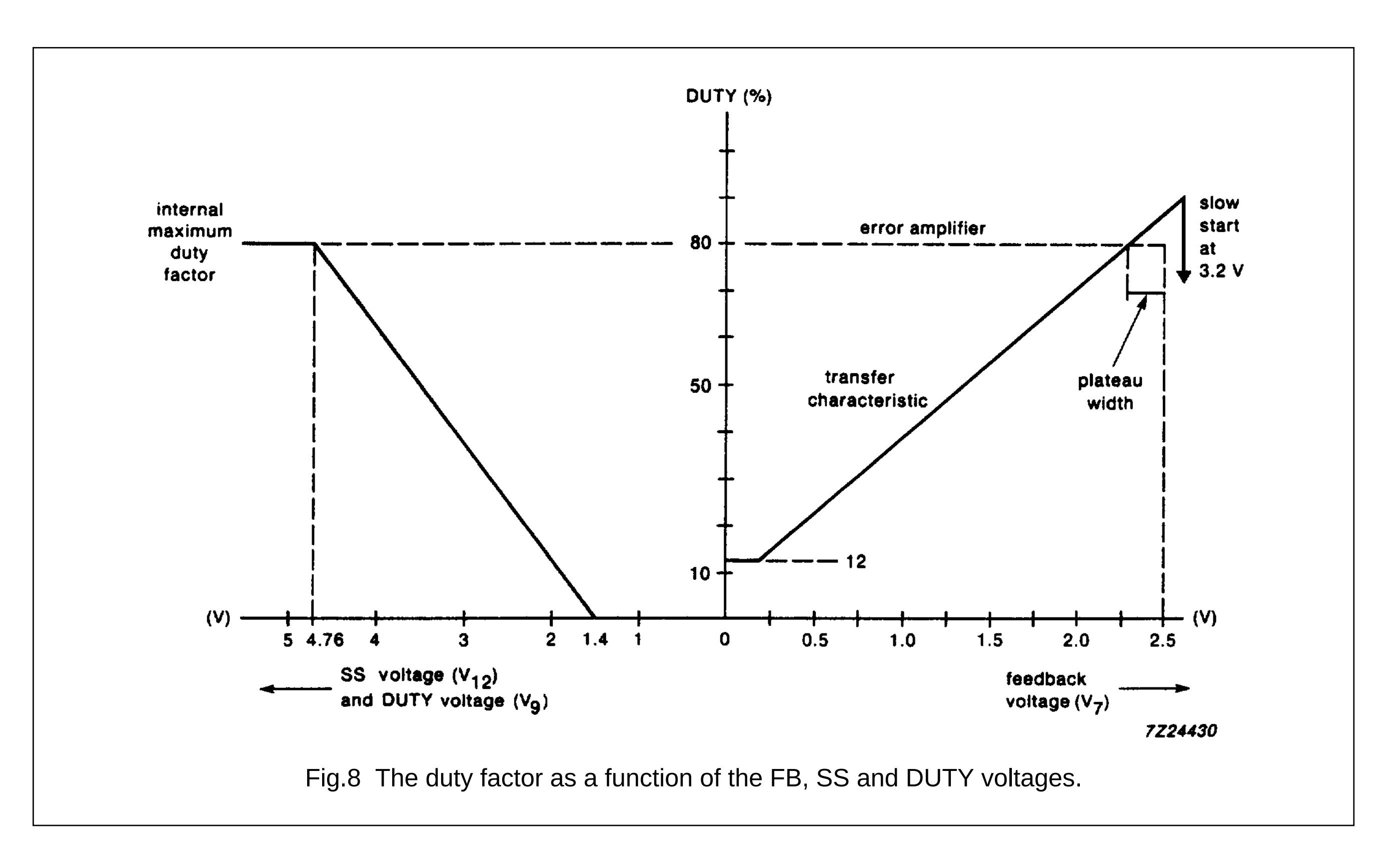


Fig.8 The duty factor as a function of the FB, SS and DUTY voltages.

Due to the characteristics of the TCG, and the fact that an open FB input results in a low voltage at the FB input, open- and short-circuit feedback loops will result in low duty factors. When DC feedback is used across the error amplifier, the current capability of the error amplifier must be considered when determining the feedback resistor value.

When the input to the PWM (pin 9) is driven by an optocoupler, the TCG can be used when a rough primary voltage is applied to the FB input. In this situation an open feedback loop will cause an increase in the FB voltage as the duty factor rises to its maximum. As soon as the FB voltage exceeds the reference by 0.7 V, the slow-start is triggered.

Demagnetization sense circuit

To enable the SMPS to be kept in the non-continuous mode, an input is available which delays switch-on of the high-voltage transistor until the transformer currents have decayed to zero. This is an effective way of avoiding transformer saturation. The waveforms illustrated by Fig.9 show demagnetization with respect to the application diagram of Fig.13.

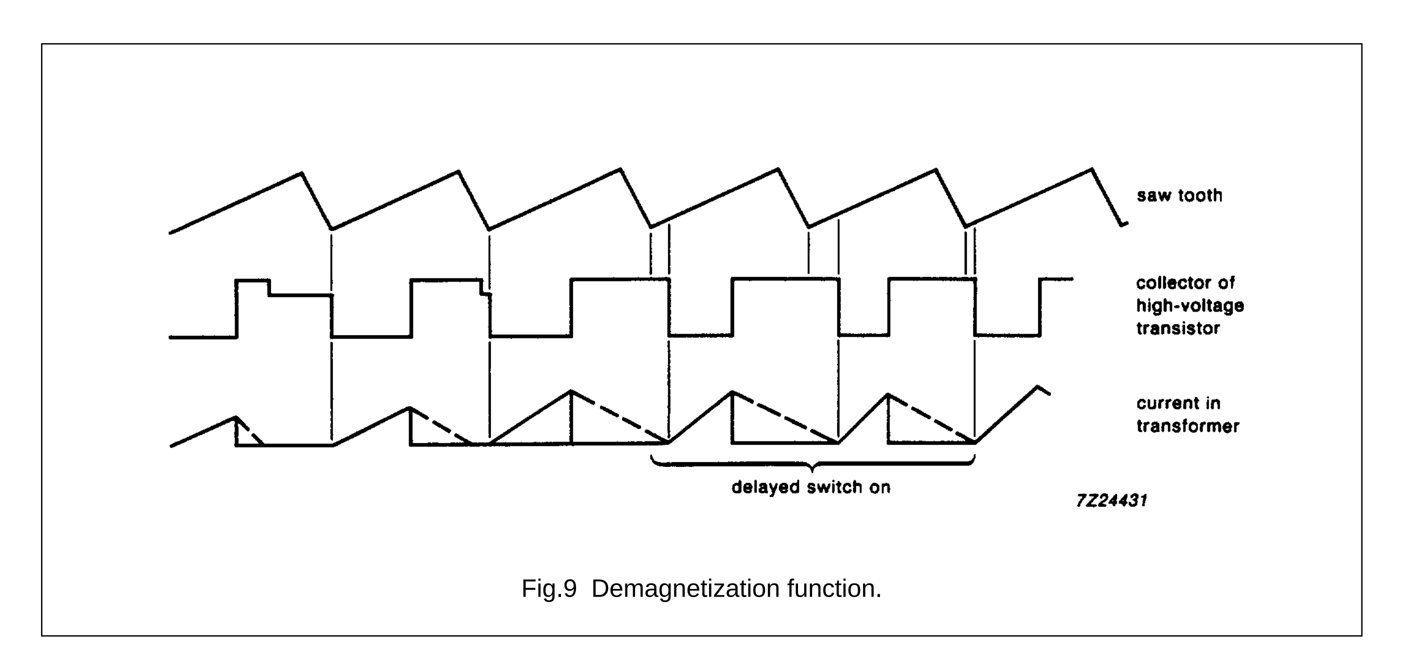


Fig.9 Demagnetization function.

As long as the voltage of the take-over (auxiliary) winding (also used for supplying the device) is above 0.6 V (V_3) the output will be prevented from switching on.

Over-current protection

The over-current protection circuit (pin 13) senses the voltage across resistor R_s (see Fig.13), which reflects the primary current. This generated voltage is negative-going as the emitter of the high-voltage power transistor is grounded (this circuit arrangement provides the IC with the best safeguard against a possible collector-emitter short-circuit in the power transistor). At pin 13, the negative voltage signal is shifted to a positive level by a voltage across resistor R_{13}. This voltage is set by the reference current at pin 13 and is defined by resistor R_6 at the I_{ref} input (pin 6) and = $1/6 \times V_{ref}/R_6$. Therefore $V_{shift}(V_{R\ 13}) = V_{ref}/6 \times R_{13}/R_6$ or nominal $0.416 \times R_{13}/R_6$ (V).

The positive current monitor voltage at pin 13 is compared with two voltage levels: the first level = 0.2 V and the second level = 0 V (see Fig.10).

The first trip level only switches off the high-voltage transistor for a cycle and puts the SMPS in a continuous cycle-by-cycle current protection mode.

The second trip level is only activated when the primary current rise is very fast which can occur during a short-circuited output. In this mode the high-voltage transistor is quickly switched off and the slow-start procedure is activated.

The difference between the first and second primary current peak levels is set by R_s:

$I_2 - I_1 = 0.2/R_s$.

The absolute peak values are set by R_6 and R_{13}:

$I_2 \times R_s = 0.416 \times R_{13}/R_6$ or
$I_1 \times R_s = (0.416 \times R_{13}/R_6) - 0.2$

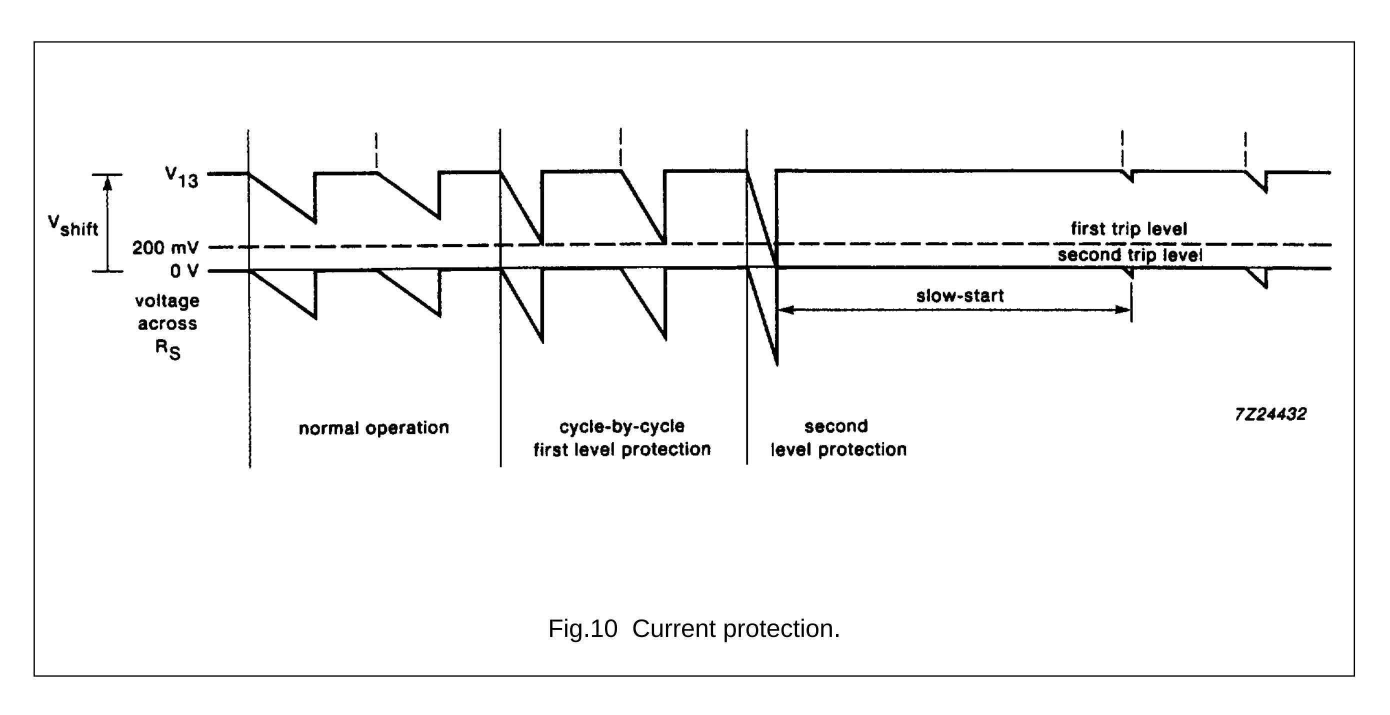


Fig.10 Current protection.

Slow-start circuit

A slow-start occurs:

- At Switch-on of the SMPS
- After a current trip as described in the section **Over-current protection**
- After a low or high V_{CC} trip.

The capacitor at the SS input is discharged and the slow-start bistable is reset when the voltage at the SS input falls below 0.5 V after which the circuit is ready for a slow-start. The dead time (during which the capacitor at the SS input is being charged to the 1.4 V lower level of the sawtooth) before duty cycle regulation starts is minimal. The SS input can also be used for D_{max} setting by connecting a resistor to ground. The voltage across this resistor is then limited to $1/6 \times V_{ref} \times R_{12}/R_6$.

Output stages

The output stage consists of two NPN darlington transistors, their collector and emitter connected to separate pins (see Fig.13). The top transistor is capable of sourcing a maximum of 0.75 A to the high-voltage transistor while the bottom transistor can sink peak currents up to 2.5 A.

For low currents up to 10 mA, the saturation voltage of the sink darlington transistor is similar to that of a single transistor (see Fig.11). During switching of this transistor dV/dt is internally limited to reduce interference.

Care should be taken with the external wiring of the output pins to avoid oscillation or interference due to parasitic inductance and wire resistance.

During start-up a small current flows from V_{CC} to E2 to precharge the series capacitor at the output (see Fig.13).

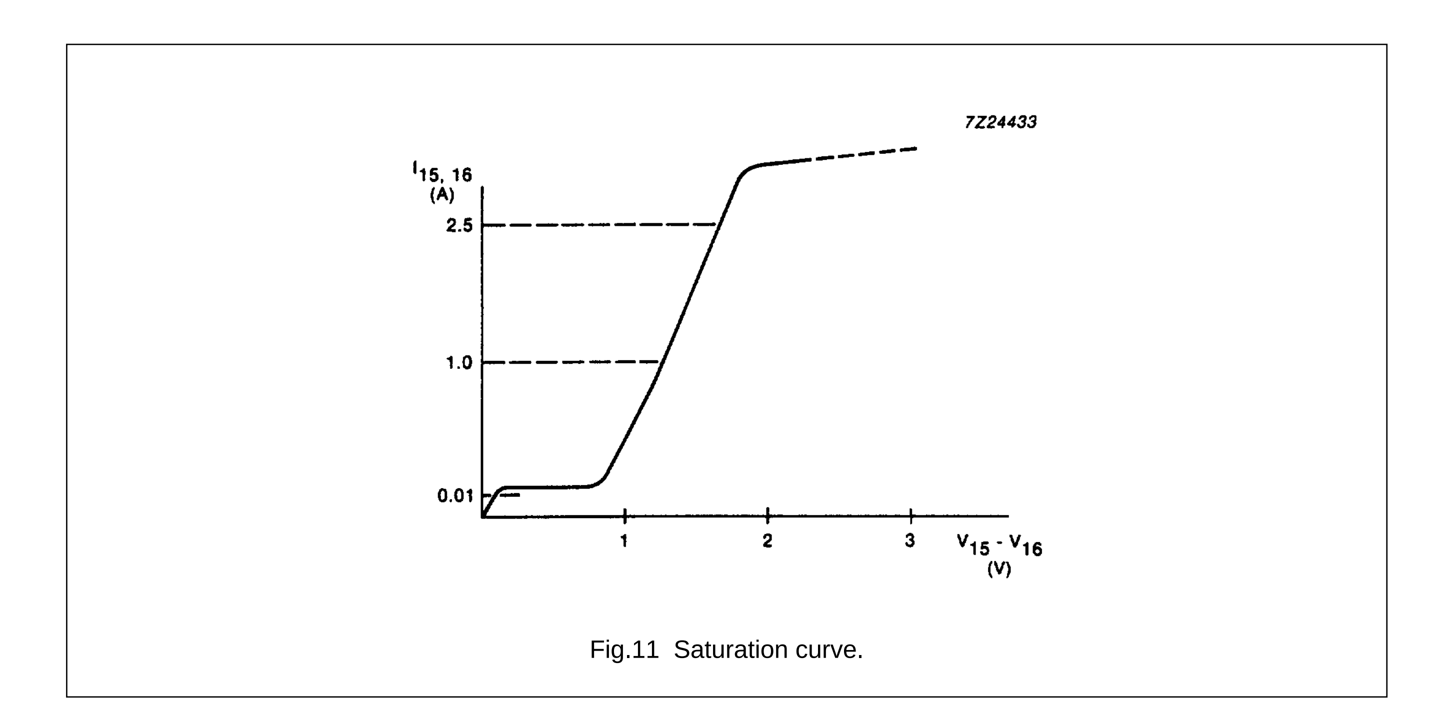


Fig.11 Saturation curve.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Voltage					
pin 5 (V_{CC})		–0.5	–	20	V
pins 1, 2, 4 and 16		–0.5	–	V_{CC}	V
pins 3 and 13		–0.5	–	0.5	V
pins 7 and 9		–0.5	–	6.5	V
pin 11		0.6	–	V_{CC}	V
Currents					
pins 5 (V_{CC})		0	–	20	mA
pin 1		–0.75	–	0	A
pin 2		0	–	0.75	A
pins 3, 4, 6 to 8 and 10 to 12		–10	–	10	mA
pin 13		–200	–	10	mA
pin 15		–2.5	–	0	A
pin 16		0	–	2.5	A
Total power dissipation	P_{tot}	see Fig.12			
Operating ambient temperature range					
(for dissipation ≤ 1 W)	T_{amb}	–25	–	+70	°C
Storage temperature range	T_{stg}	–55	–	+150	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j-a(max)}$ = 55 K/W

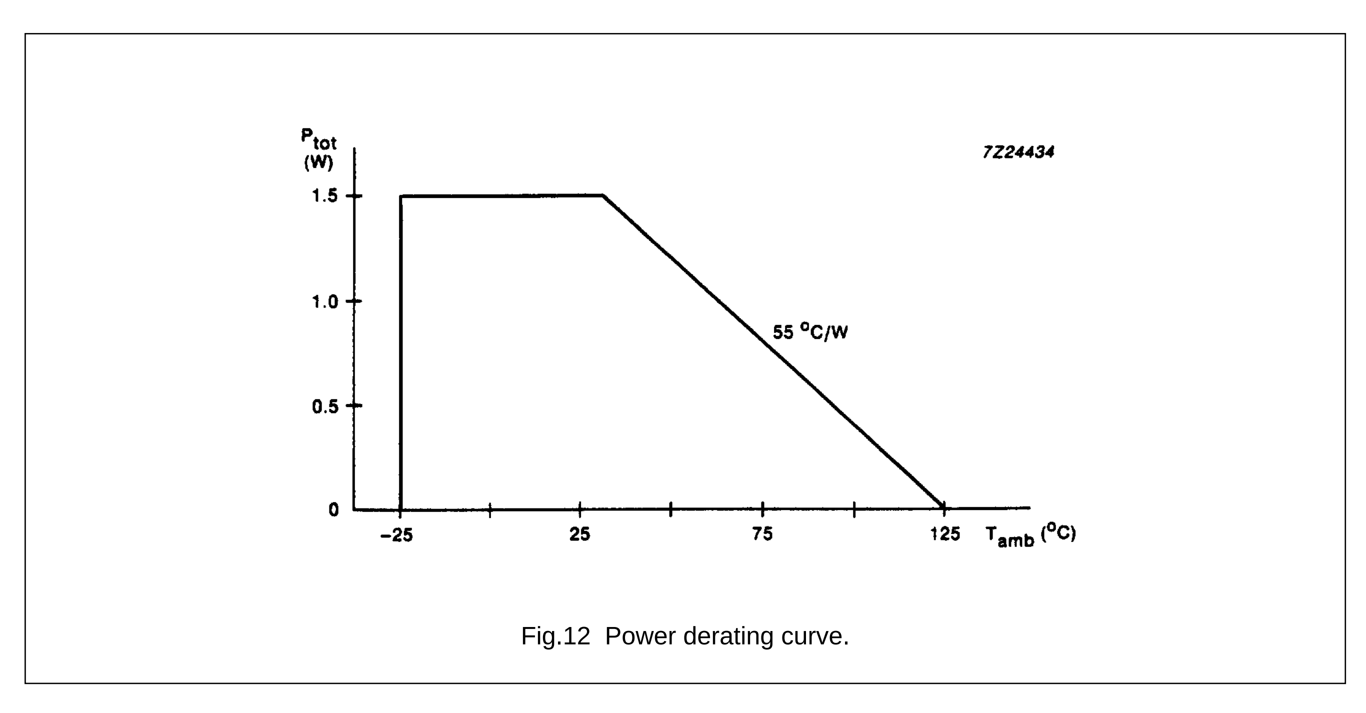


Fig.12 Power derating curve.

CHARACTERISTICS

V_{CC} = 14 V; T_{amb} = 25 °C; reference resistor = 5 kΩ unless otherwise specified

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply						
Supply voltage		V_{CC}	9	–	20	V
Supply initialization level		V_5	15	17	18	V
High voltage protection		V_5	21	23	25	V
Internal fixed minimum protection level		V_5	7.9	8.4	8.9	V
Hysteresis		dV_{CC}	–	50	–	mV
Supply current						
operational		I_{CC}	–	–	15	mA
before initialization		I_{CC}	–	100	150	μA
Reference current (pin 4)	note 1	I_4	$I_6/5.7$	$I_6/6$	$I_6/6.4$	mA
Trigger level V_{CCmin} setting		V_5	$3.6V_4$	$3.8V_4$	$4.2V_4$	V
Clamp voltage	at 20 mA		21.5	23.5	25.5	V
Reference (pin 6)						
Reference voltage		V_{ref}	2.4	2.5	2.6	V
Current range		I_{ref}	200	–	800	μA
Reference voltage over I_6 range		dV_{ref}	–20	–	+ 20	mV
Error amplifier						
Error amplifier threshold	V_{CC} = 8.5 to 20 V	V_7	2.4	2.5	2.6	V
Input current		I_7	0	–	5	μA
Sink current output	at 1.2 V	I_8	1	–	–	mA
Source current output	at 5.5 V	I_8	80	100	130	μA
Open loop gain		A0	–	100	–	dB
Unity gain bandwidth		BW	–	5	–	MHz
Input DUTY current	note 1	I_9	$I_6/5.7$	$I_6/6$	$I_6/6.3$	mA
High FB protection level		V_7	2.95	3.1	3.25	V
Temperature coefficient of error amplifier threshold		dV_7/dT	–	100	–	10^{-6}/K
TCG function (see Fig.8)						
Transfer characteristics		dD/dV_7	–	32	–	%/V
Minimum duty factor		D_{min}	–	12	–	%
Plateau width		V_7	–	200	–	mV

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Slow-start function						
Transfer characteristics		dD/dV_{12}	–	23.8	–	%/V
Input current	note 1	I_{12}	$I_6/5.7$	$I_6/6$	$I_6/6.3$	mA
Sink current during faults	at 0.5 V	I_{12}	8	–	–	mA
Internally fixed maximum duty factor		D_{max}	75	80	85	%
Clamp current	at V_{12} = 0.5 V	I_{12}	–	–2	–	mA
Output stage						
Source transistor						
Voltage drop with respect to V_{CC}	at 0.75 A	$V_{CC}–V_1$	–	2	–	V
Pull-up current	$V_{CC} – V_1$ = 15 V	$–I_1$	25	–	100	μA
Operating current range		$–I_1$	0	–	0.75	A
Sink transistor (see Fig.11)						
Saturation voltage						
at 2.5 A		$V_{16} – V_{15}$	–	2	–	V
at 1 A		$V_{16} – V_{15}$	–	1.5	–	V
at 10 mA		$V_{16} – V_{15}$	–	0.3	–	V
Leakage current	$V_{16} – V_{15}$ = 20 V	I_{16}	–	–	1	μA
Falling edge		$dV_{16–15}/dt$	–	0.2	–	V/ns
Operating current range						
Peak		I_{16}	0	–	2.5	A
Average		I_{16}	–	–	250	mA
Oscillator						
High level voltage		V_{10}	–	5	–	V
Low level voltage		V_{10}	–	1.4	–	V
Charge current	note 1	I_{10}	$I_6/5.7$	$I_6/6$	$I_6/6.3$	mA
Frequency range		f_o	10	–	100	kHz
Frequency	R_6 = 5 kΩ C_{10} = 680 pF	f_o	27	28.5	30	kHz
Temperature coefficient of the frequency		df/dT	–	100	–	$10^{–6}$/K

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Synchronization						
Minimum synchronization pulse width		t_{11}	–	–	0.5	μs
Switching threshold		V_{11}	0.7	0.85	0.9	V
Input current		I_{11}	2.5	5.0	7.5	μA
Disabling threshold		V_{11}	4.2	5.6	6.0	V
Input voltage	at –700 μA	V_{11}	390	–	550	mV
Demagnetization input						
Switching voltage level		V_3	615	645	675	mV
Switching current level		I_3	–23	–	–39	μA
Current range of clamp circuits		I_3	–10	–	+ 10	mA
Clamp level positive	at 10 mA	V_3	–	950	–	mV
Clamp level negative	at –10 mA	V_3	–	–800	–	mV
Temperature coefficient		TC	–	–1.9	–	mV/K
Current protection						
Input current	note 1	I_{13}	I_6/5.7	I_6/6	I_6/6.3	mA
First threshold		V_{13}	190	200	210	mV
Second threshold		V_{13}	–10	0	10	mV
Delay to switch output via level 1	pulse at pin 13 from 300 mV to 100 mV; I_O = 500 mA	–	–	350	–	ns
Delay to switch output via level 2	pulse at pin 13 from 300 mV to –200 mV; I_O = 500 mA	–	–	300	500	ns
First threshold including R_{13} (12 kΩ)	R_6 = 5 kΩ	–	–	–800	–	mV
Threshold for open pin detection		V_{13}	–	3.5	–	V

Note to the characteristics

1. Over the current range of I_6; 200 to 800 μA.

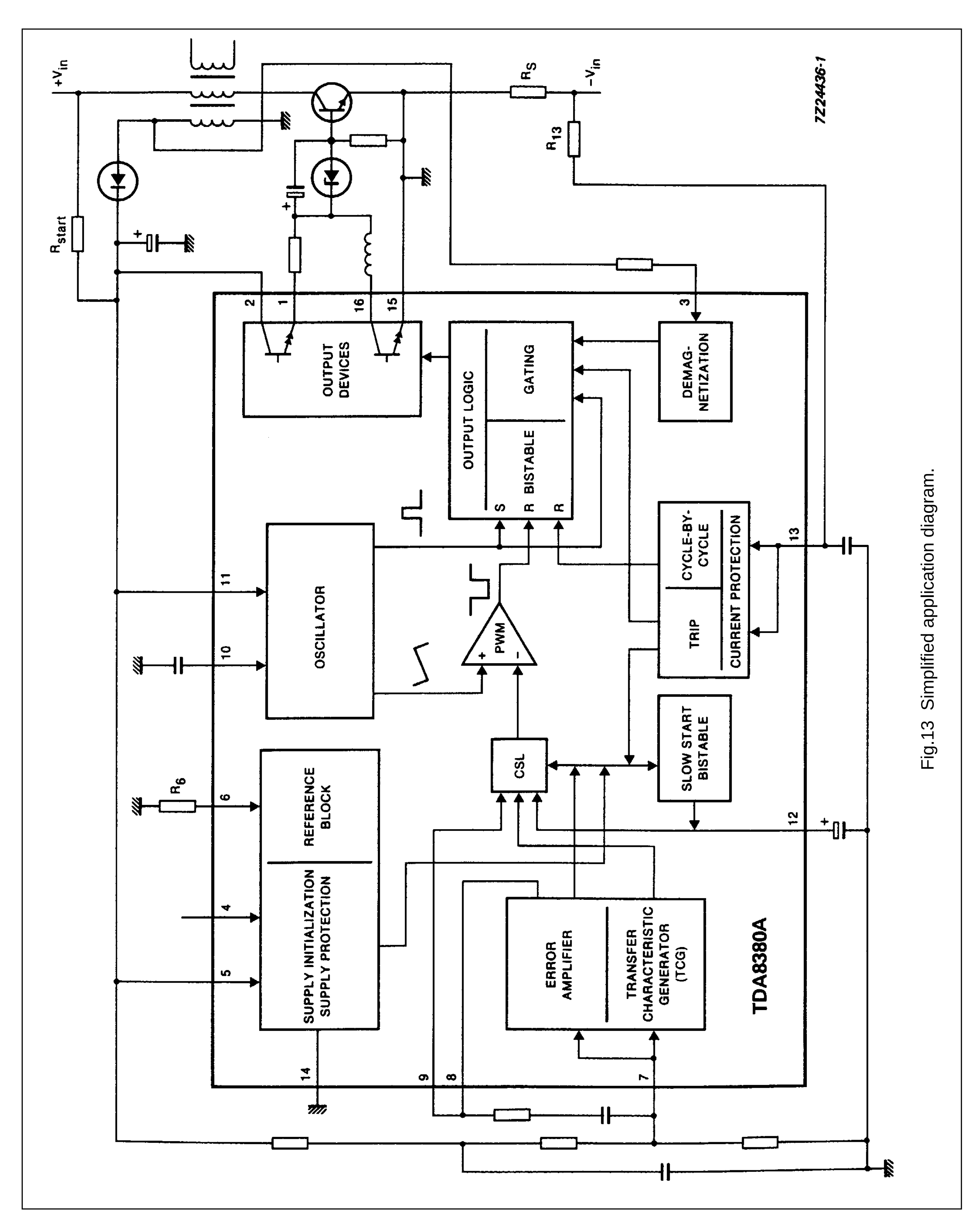


Fig.13 Simplified application diagram.

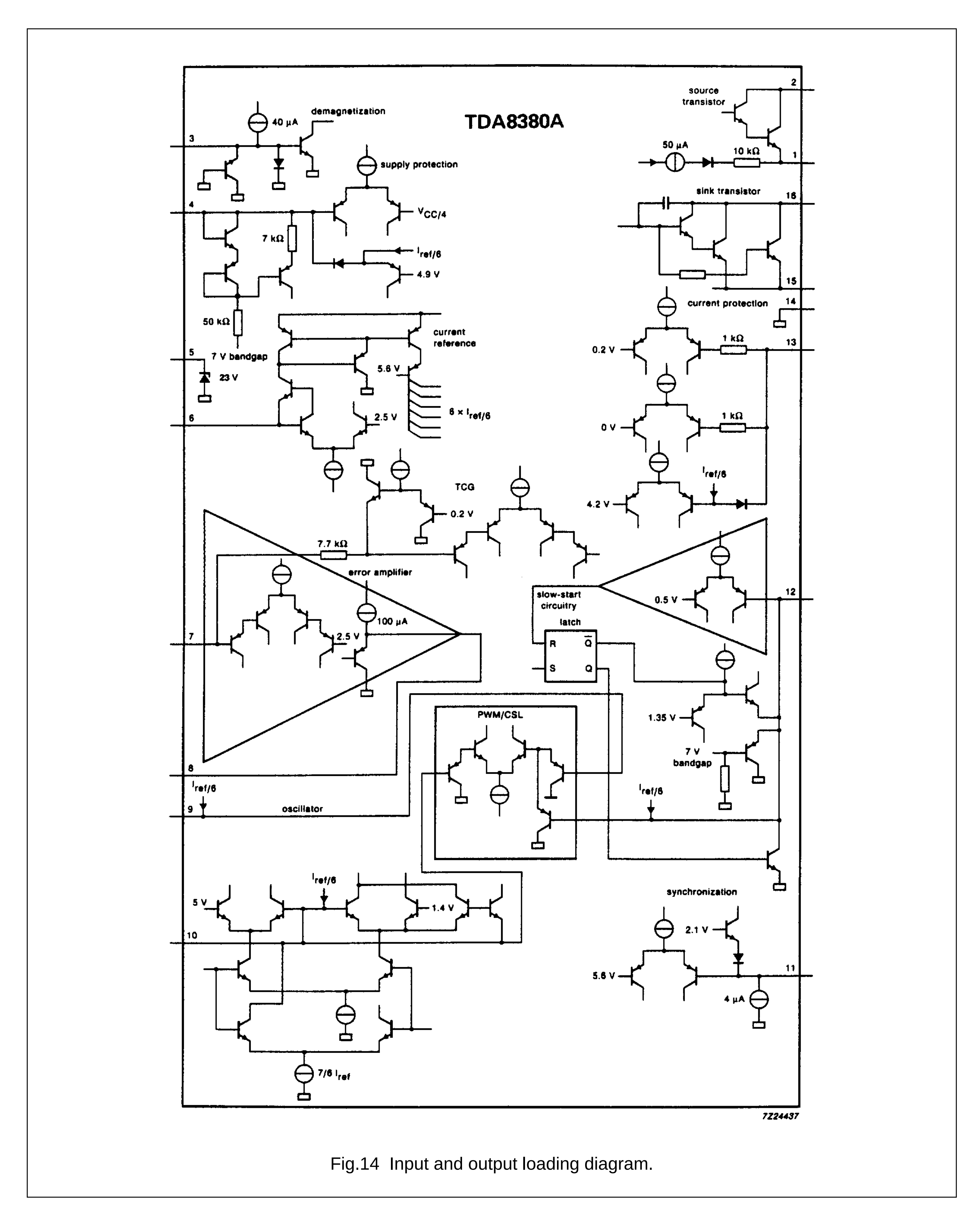
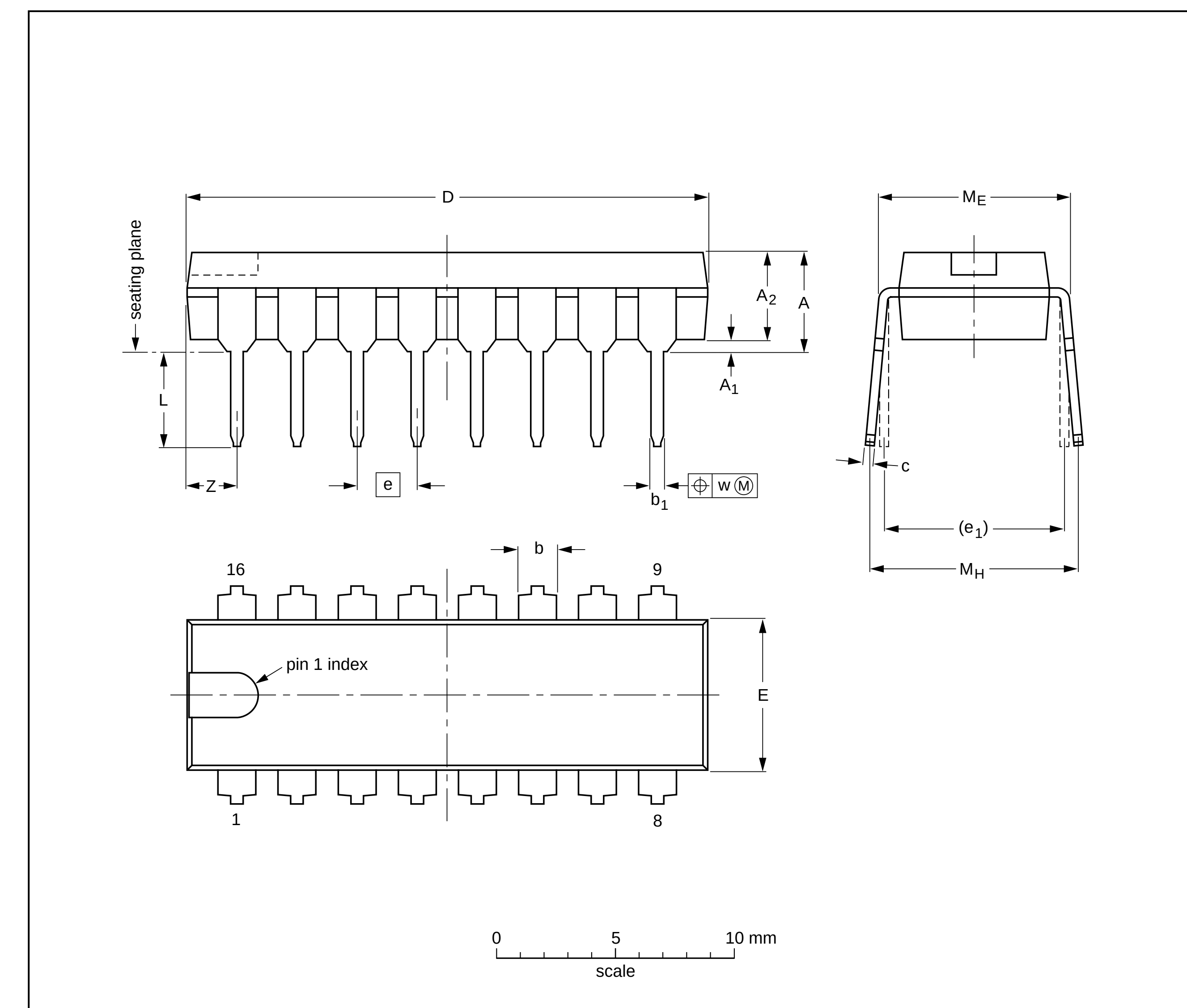


Fig.14 Input and output loading diagram.

PACKAGE OUTLINE

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.